High-density HTS interconnects with ultra-low thermal loss

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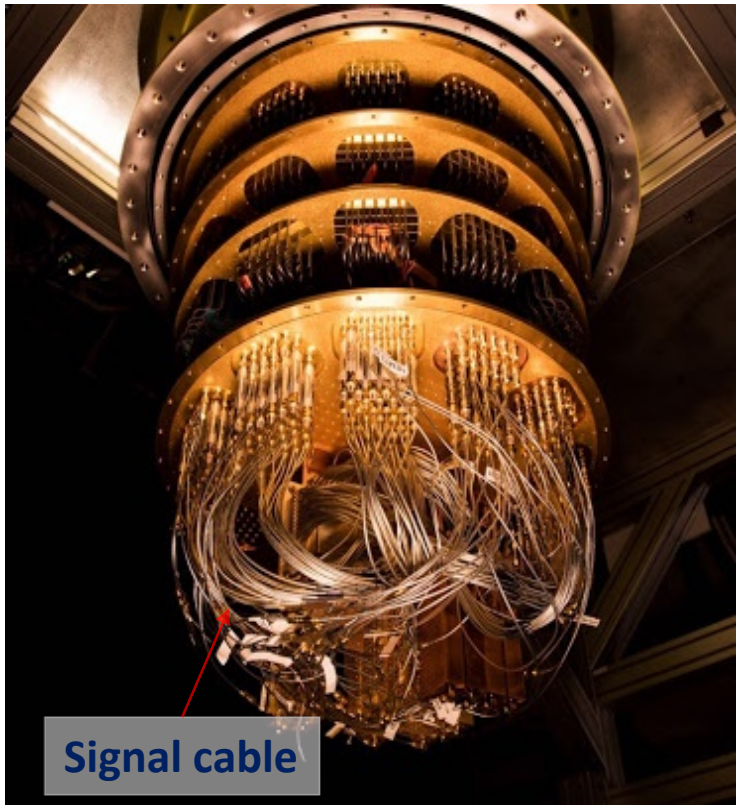
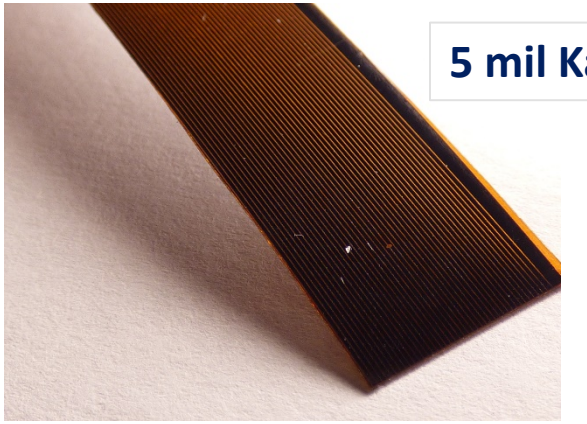
Motivation: practical quantum computers would need 1,000's of interconnects

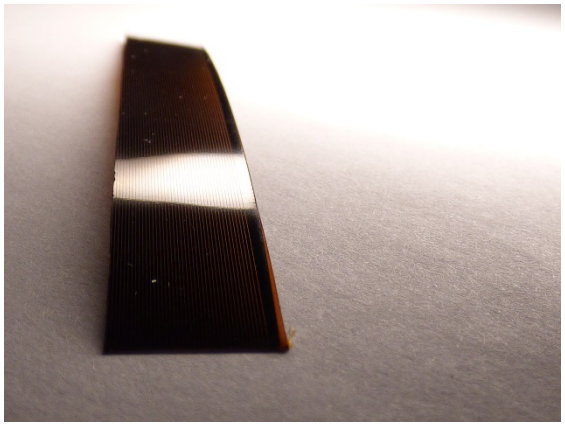
Existing IBM system

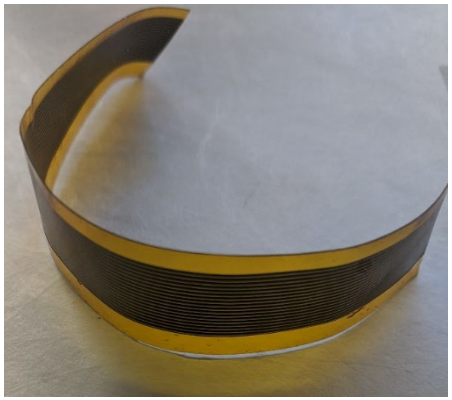


Solution: **high density superconducting cable With ultra-low thermal loss**



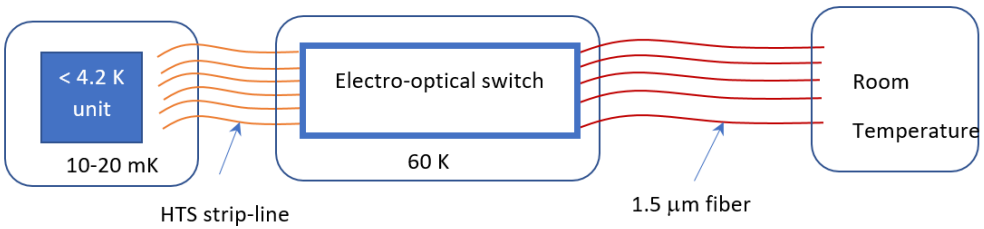
5 mil Kapton

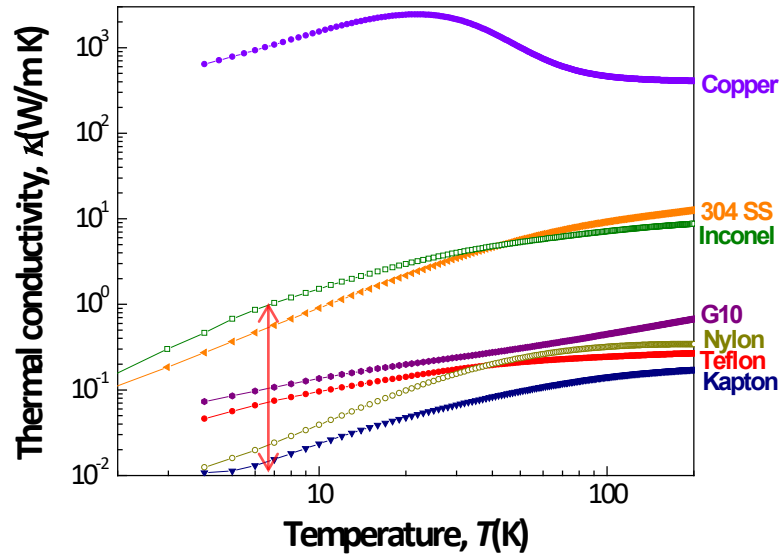




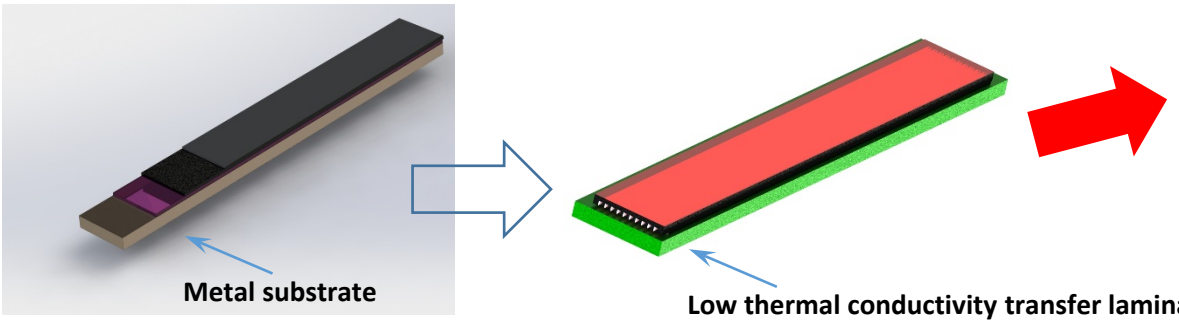
1 mil Kapton

Solution: exfoliated HTS striplies





- **HTS can work between 60 K and < 100 mK**
- **However the substrate (metal) will generate high thermal loss**



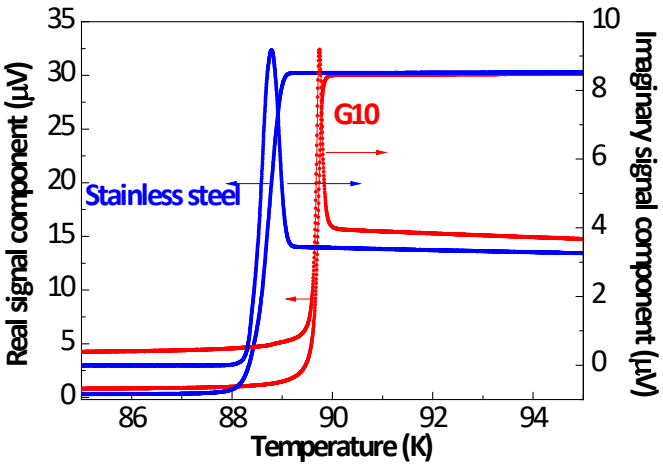
x100 reduction of thermal loss

✓ **By transferring epitaxial HTS layer to a low-loss dielectric we reduce the thermal loss by x100, impossible with Wiedemann-Franz metals**

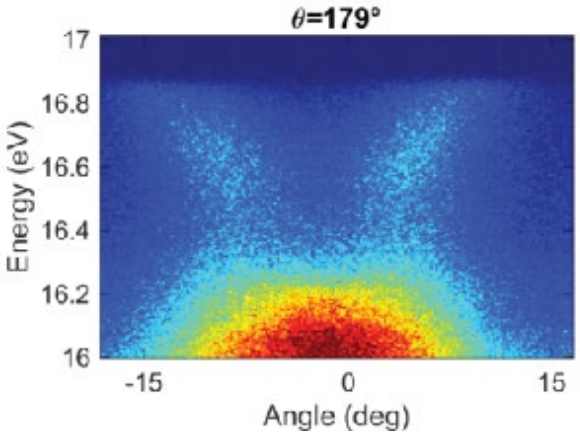
✓ **Data transfer from 60-70 K can be efficiently accomplished by off-shelf Si opto-electronics**

Advantages of the exfoliated YBCO-Kapton

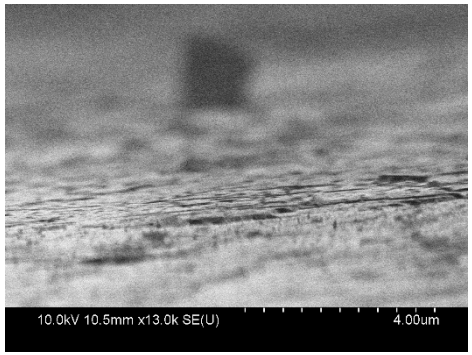
High Tc (due to compression)



High carrier density (substrate side)



Smooth surface



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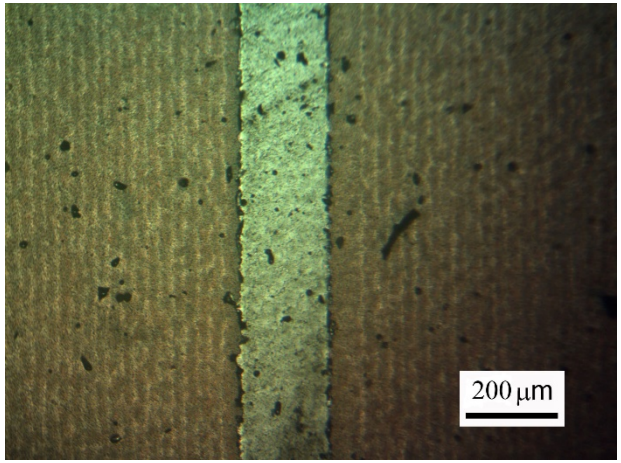
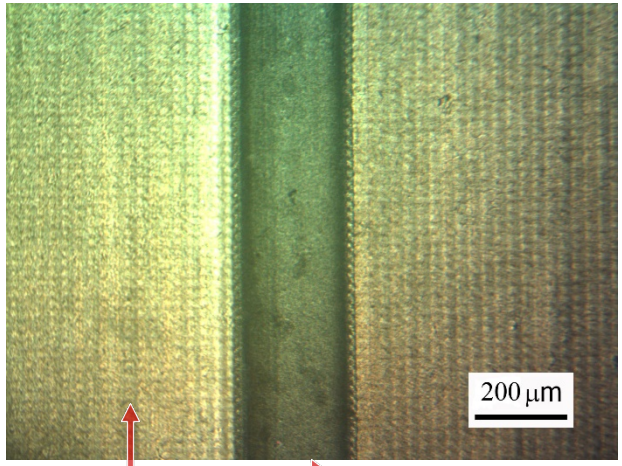
Narrow line patterning for high-density striplines

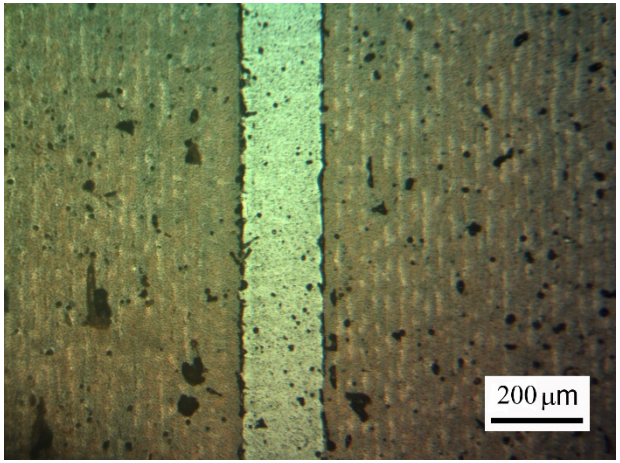
-1 mm



Optimum, in focal plane

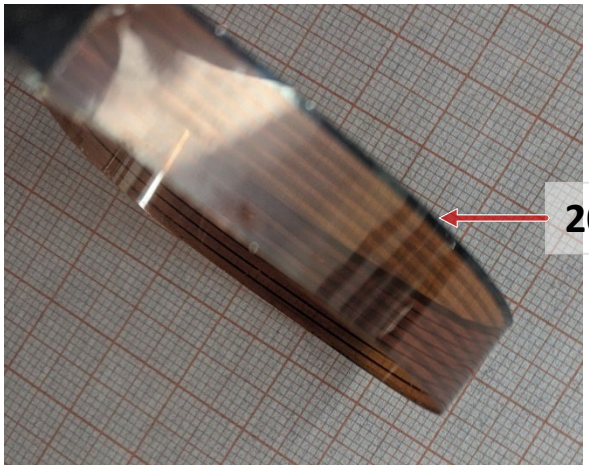


+1 mm



5 mil Kapton

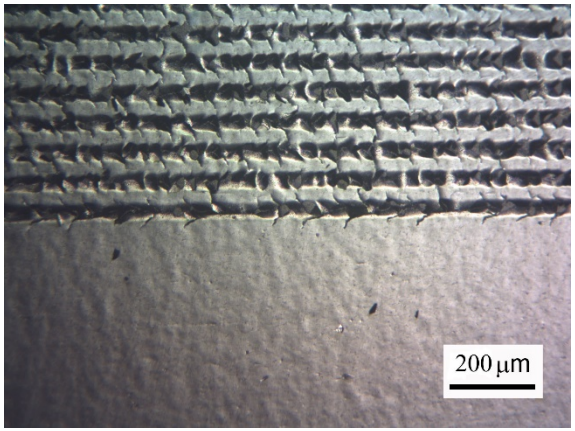
1 μm YBCO



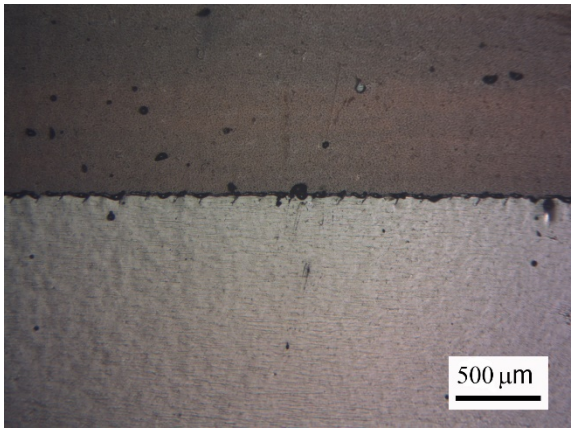
200 mm wide YBCO lines on 5 mil Kapton

Optimization of laser patterning and compression level

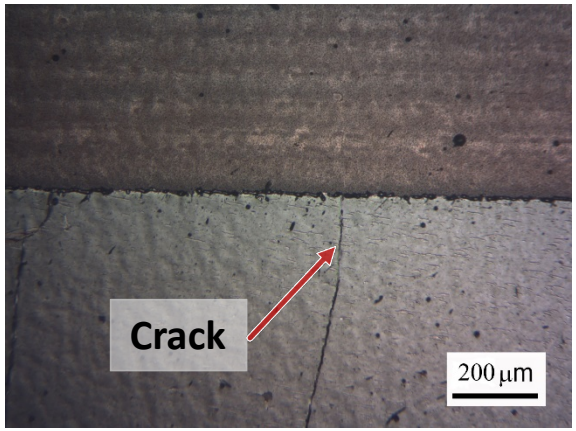
7 W

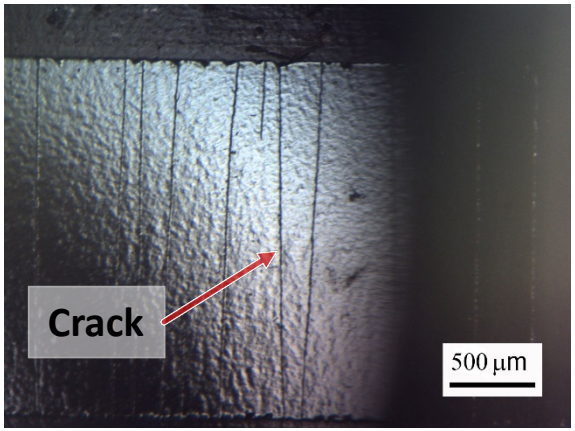


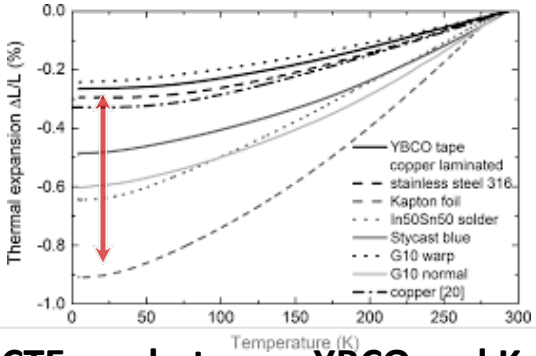
15 W, optimum power



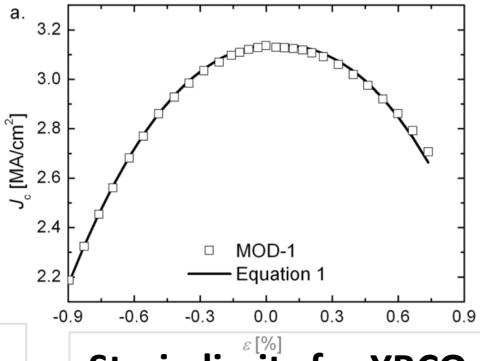
30 W







CTE gap between YBCO and Kapton

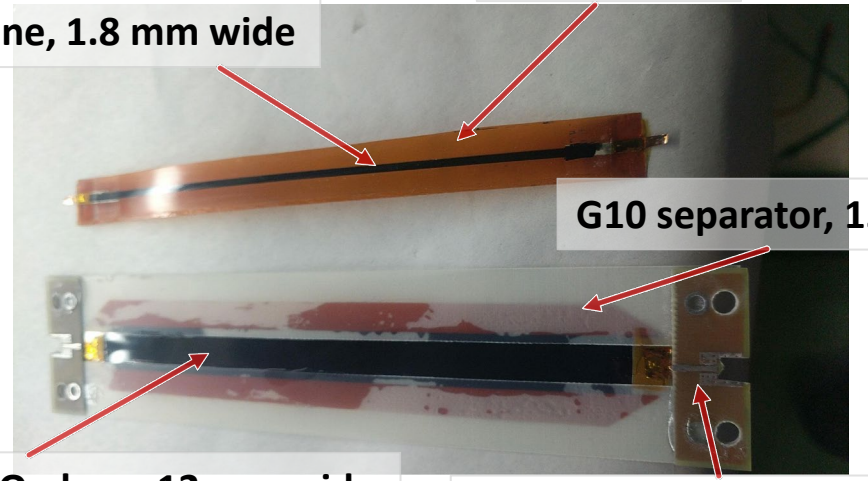


Strain limits for YBCO

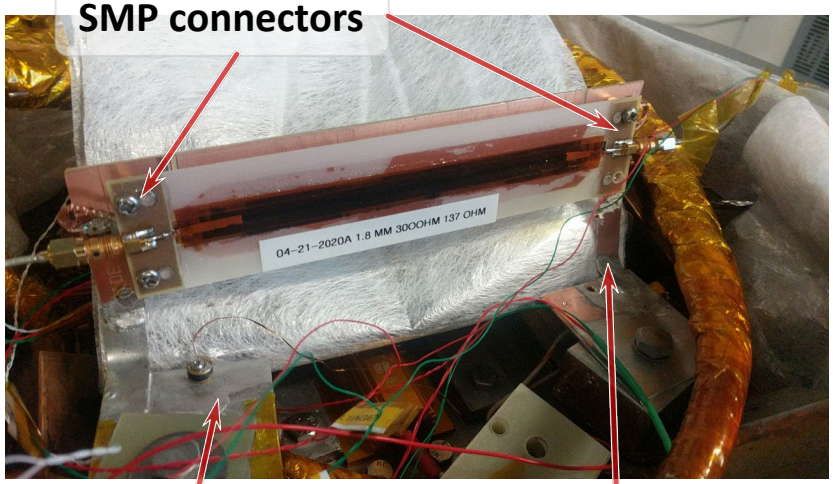
✓ **Careful managing of thermal effects level is critical**

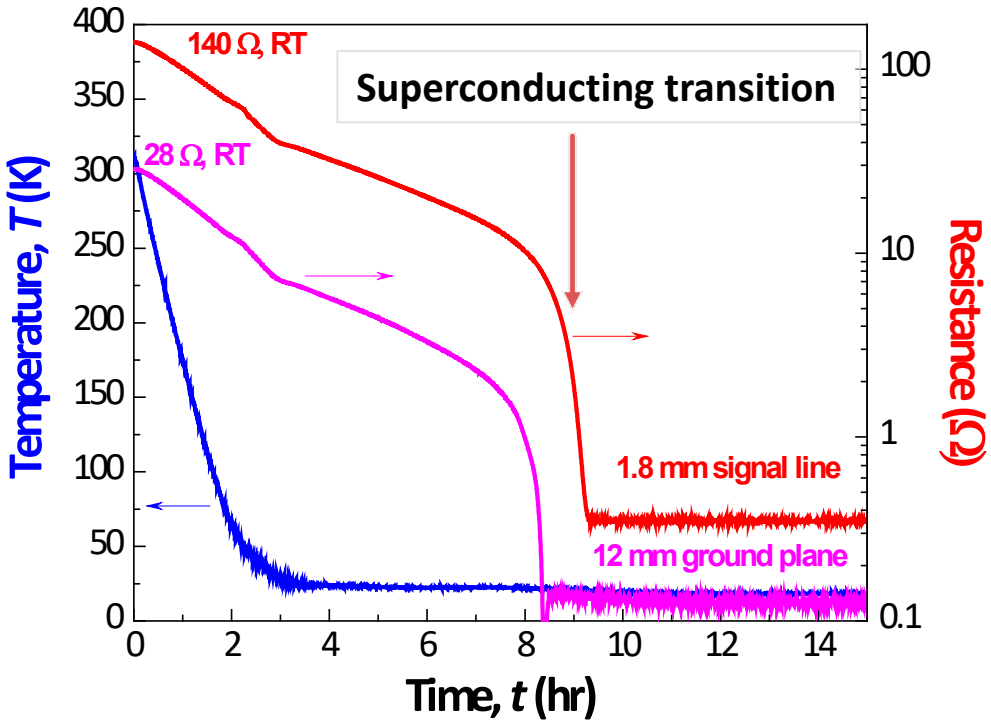
Air-gapped YBCO-on-Kapton microstrip

- 0.33 mm air gap, $\varepsilon = 1$
- 15 cm long
- Projected 50 Ω impedance at 1.8 mm
- Ground plane: 32 Ω at RT
- Signal line 149 Ω at RT



Air-gapped microstrip test, in vacuum conduction cooling





✓ Approx. 3 hours equilibration time

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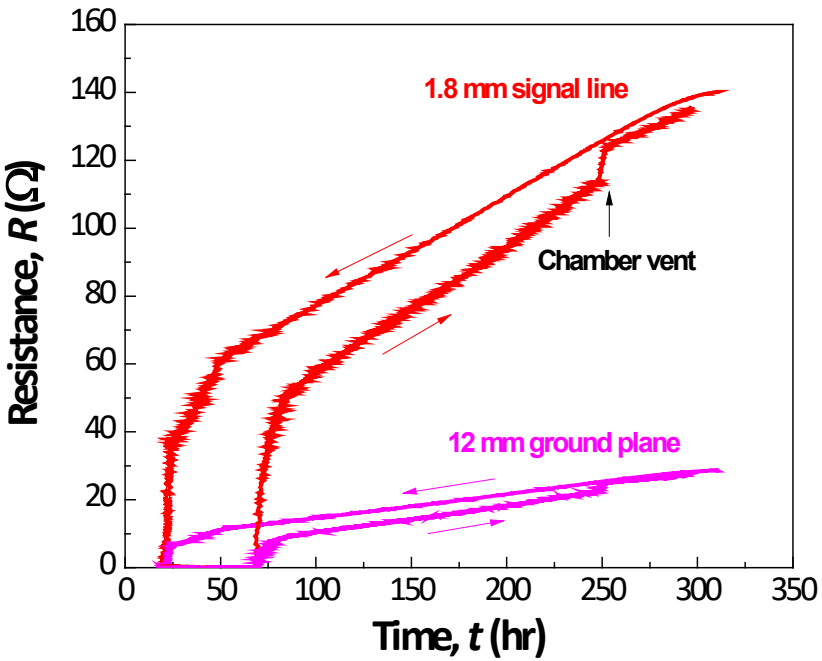
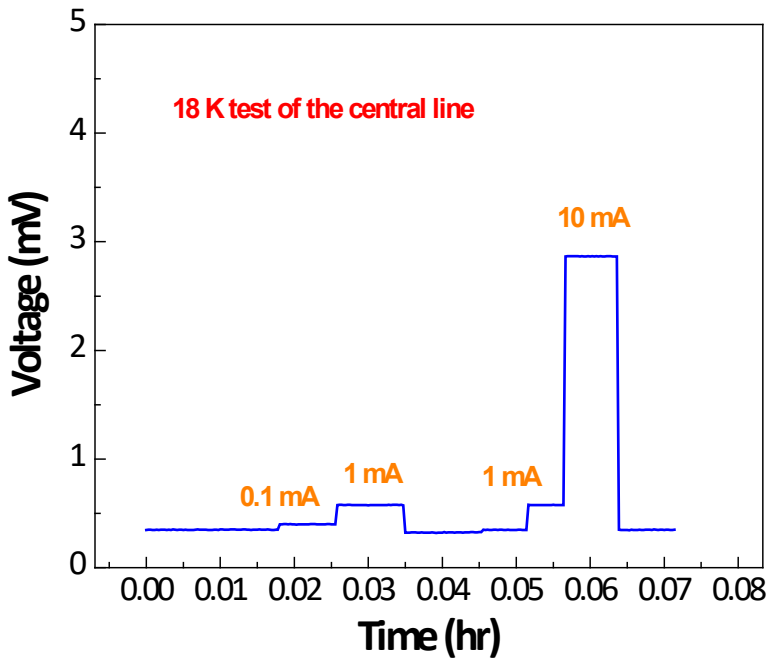
18 K - RT cycling of the air-gapped microstrip



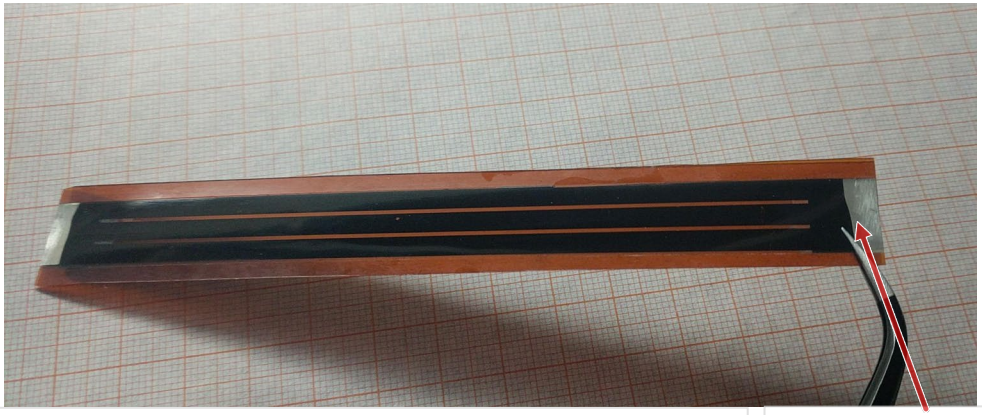


- ✓ The assembly sustained 5 cycles from 18 K to room temperature
- ✓ Central line sustained up to 10 mA current at 18 K

Dielectric YBCO-on-Kapton microstrip

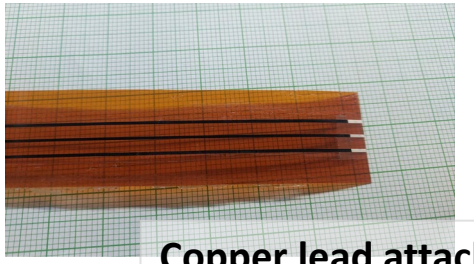
- 0.33 mm thick dielectric, $\varepsilon = 3.2$
- 12 cm long
- Projected 50 Ω impedance at 0.8 mm
- 3 lines 3 mm apart

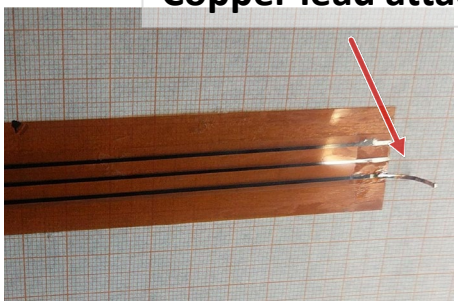
Ground plane side, 33 Ω RT



Signal line side, 0.8 mm wide lines, 500 – 600 Ω RT

Metallization

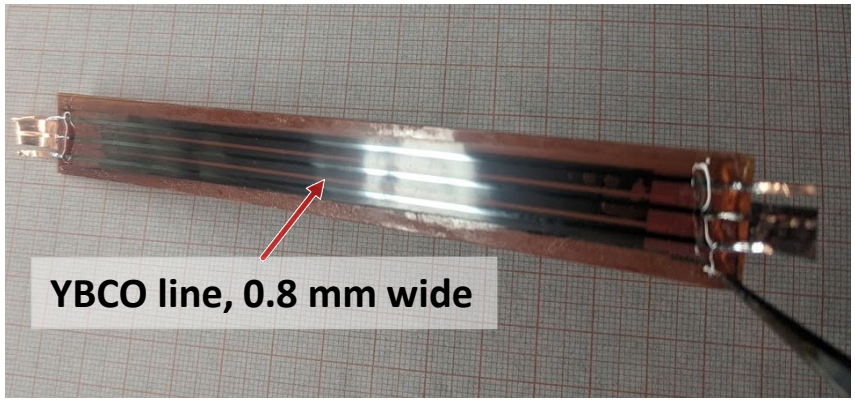




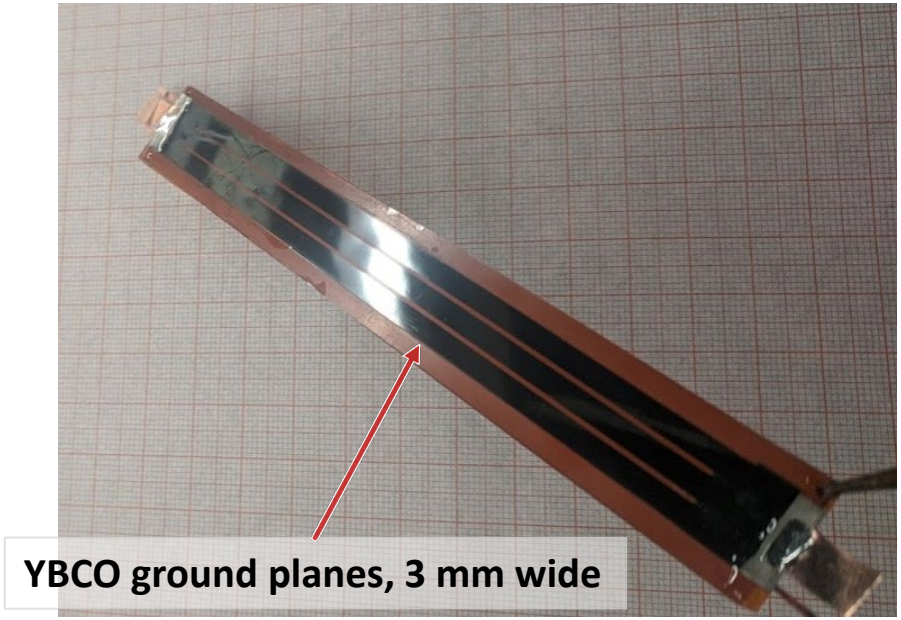
Copper lead attached

Assembled dielectric YBCO-on-Kapton microstrip

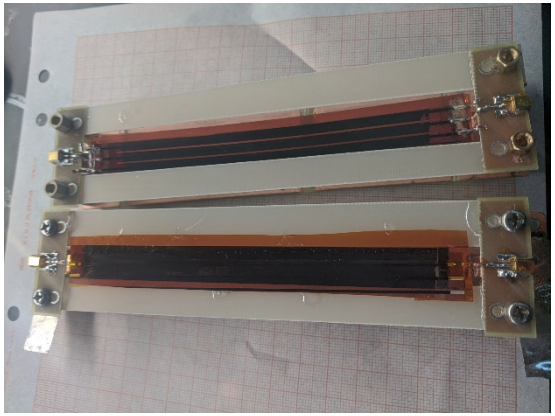
Signal plane side



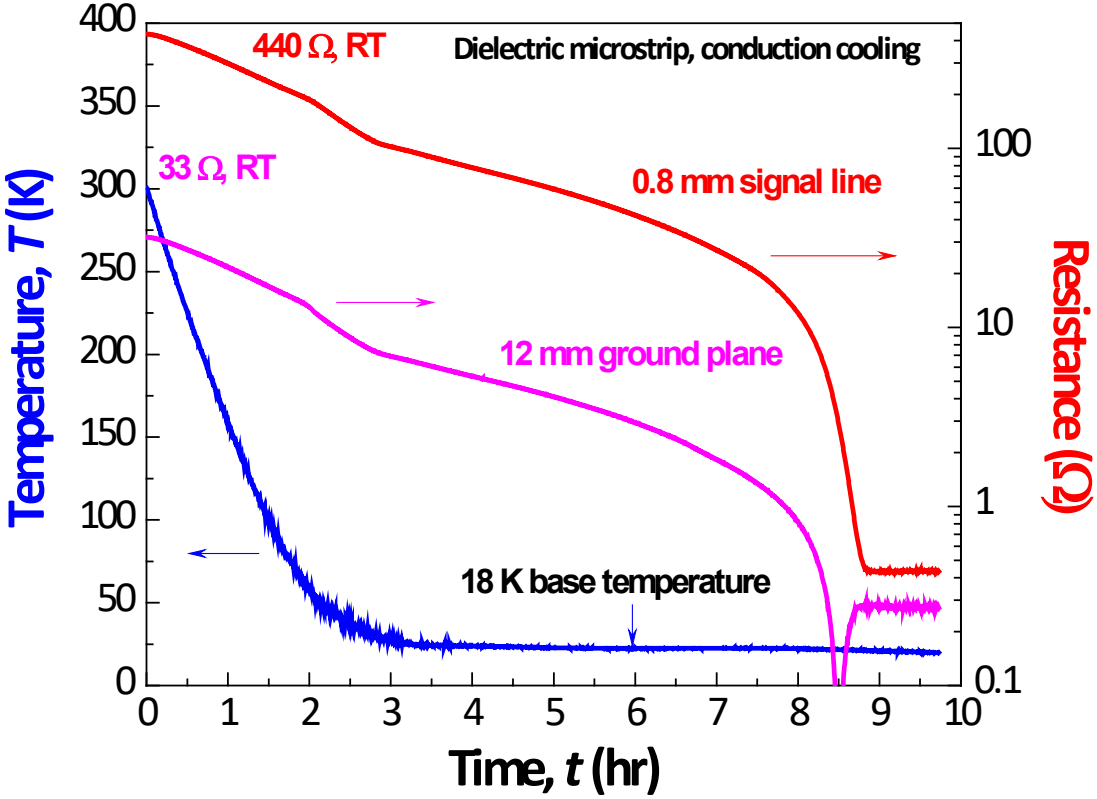
Ground plane side



Assembled microstrips



Conduction cooling test of the dielectric microstrip

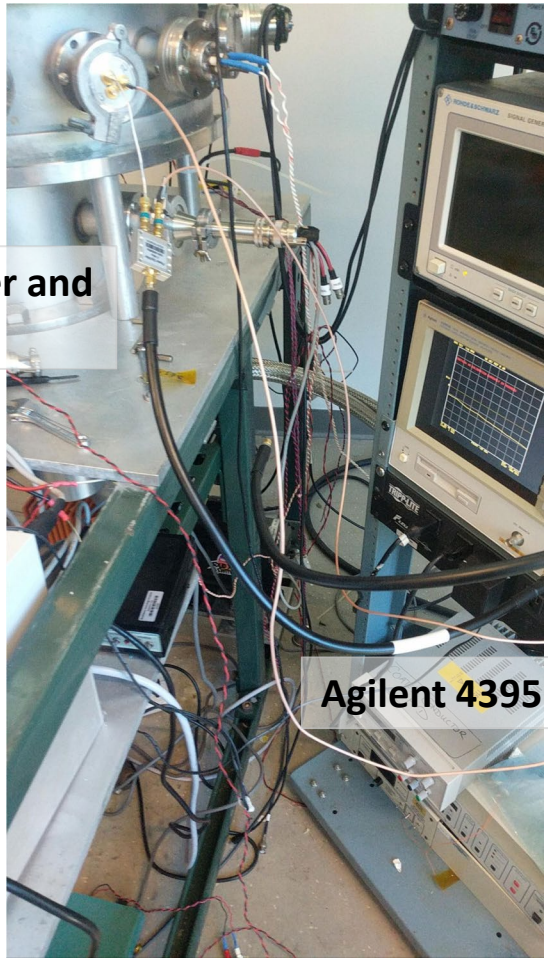


- ✓ The assembly sustained 5 cycles from 18 K to room temperature
- ✓ Central line sustained up to 10 mA current at 18 K

Experiment

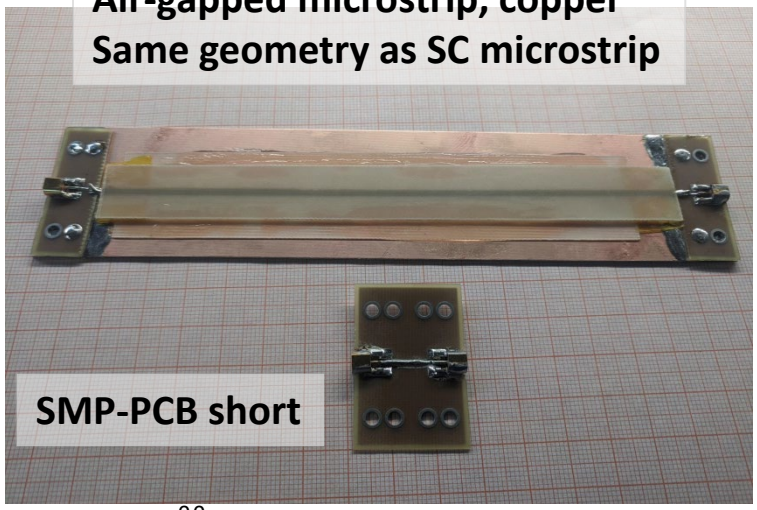
Cryochamber

Power splitter and attenuators

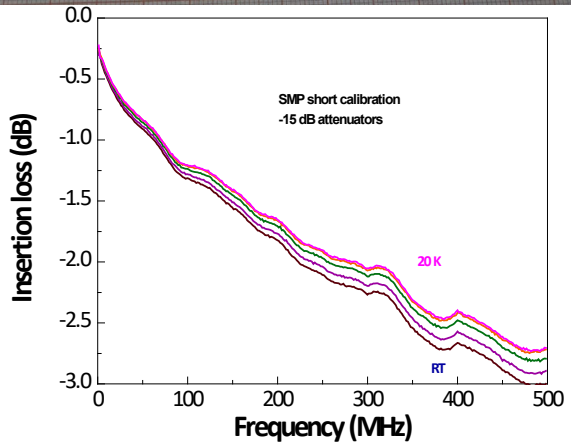


Agilent 4395 A VNA

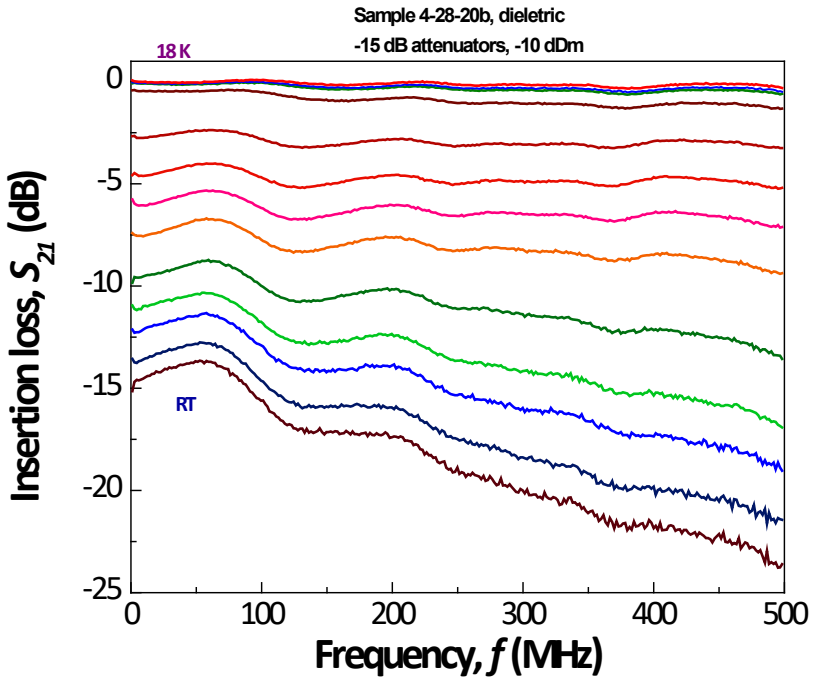
Air-gapped microstrip, copper
Same geometry as SC microstrip

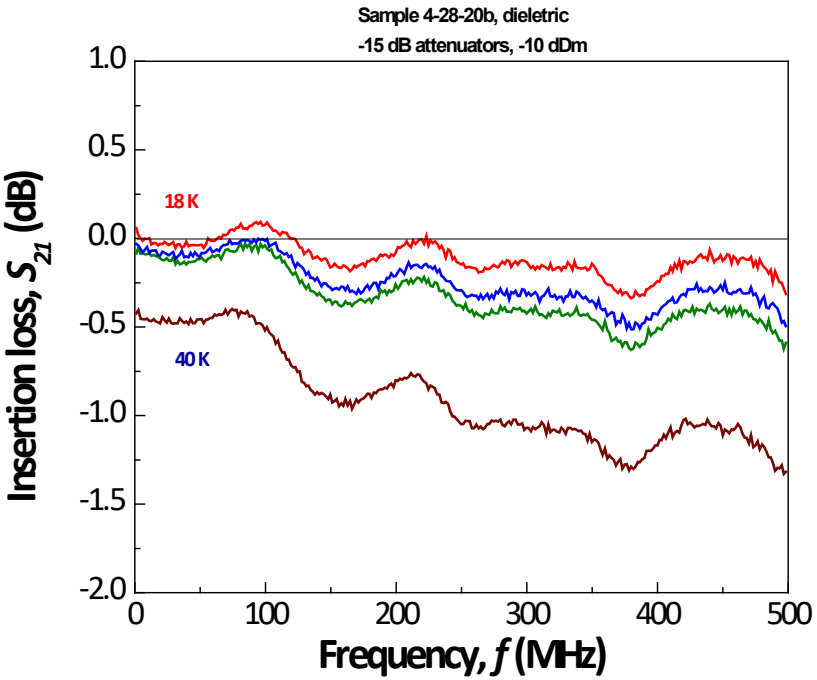


SMP-PCB short



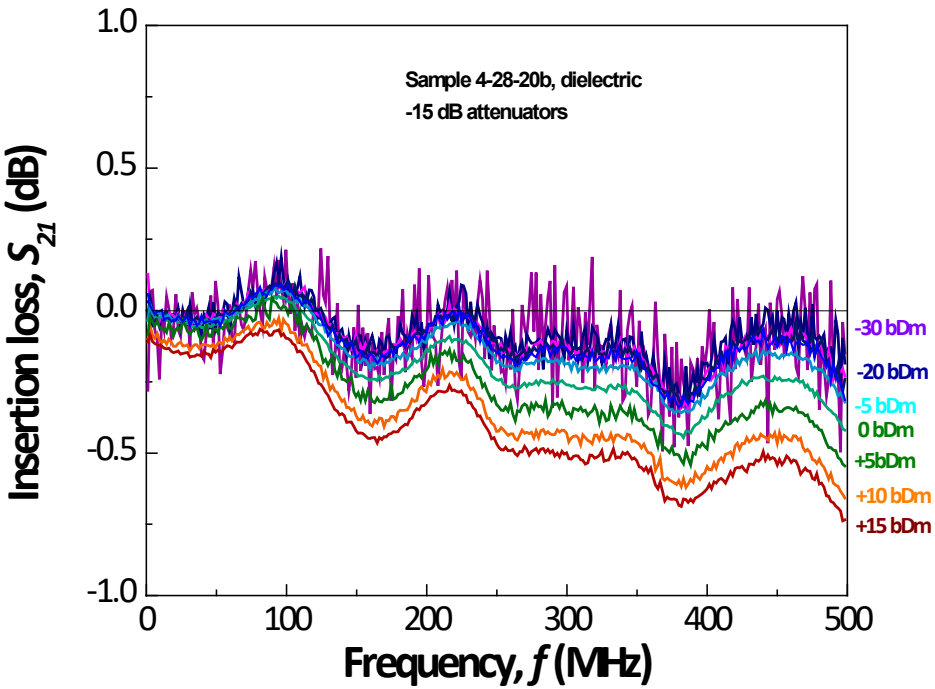
Successful conduction cooled test: dielectric microstrip

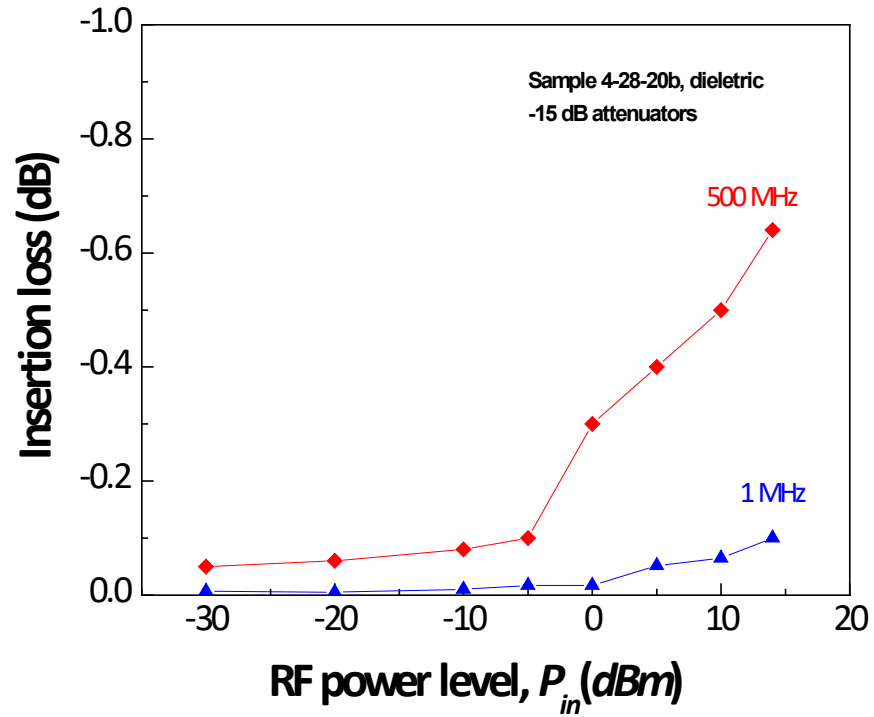




✓ **Insertion loss ≈ 0.1 dB at 500 MHz at 18 K**

Power dependence of the loss

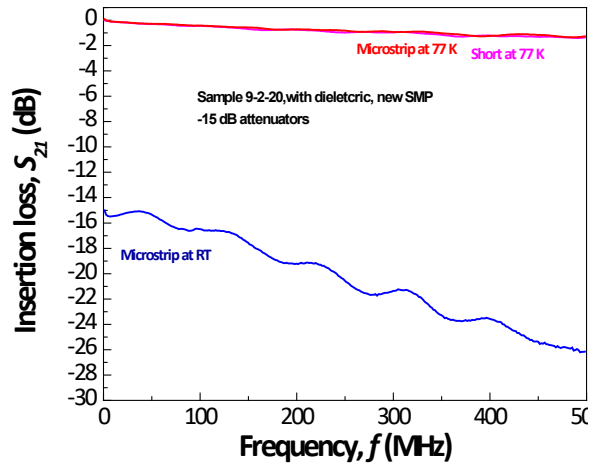


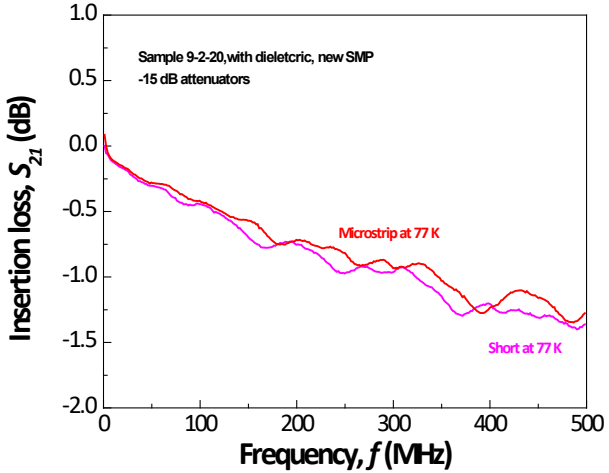


✓ **Mechanism of the power dependence needs to be further investigated**

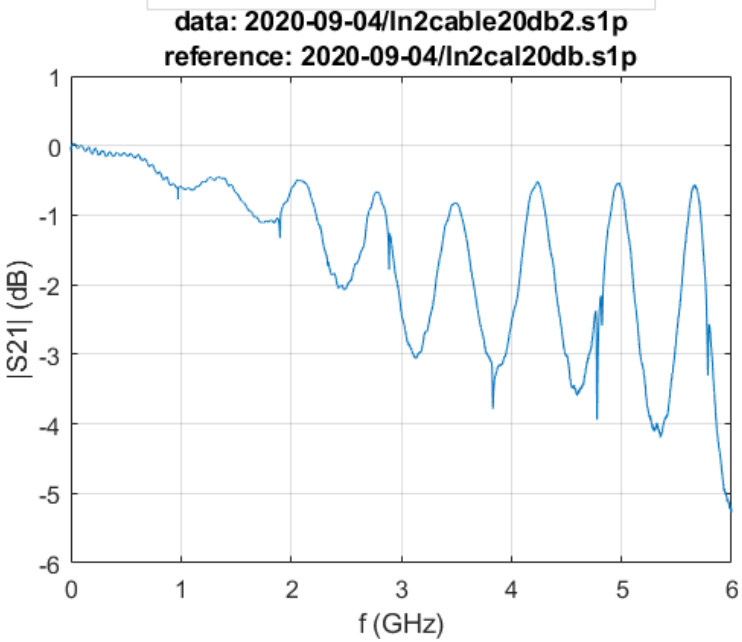
Right-angle launch SMP dielectric line test at 77 K: improved connector design

Up to 500 MHz test at BTG



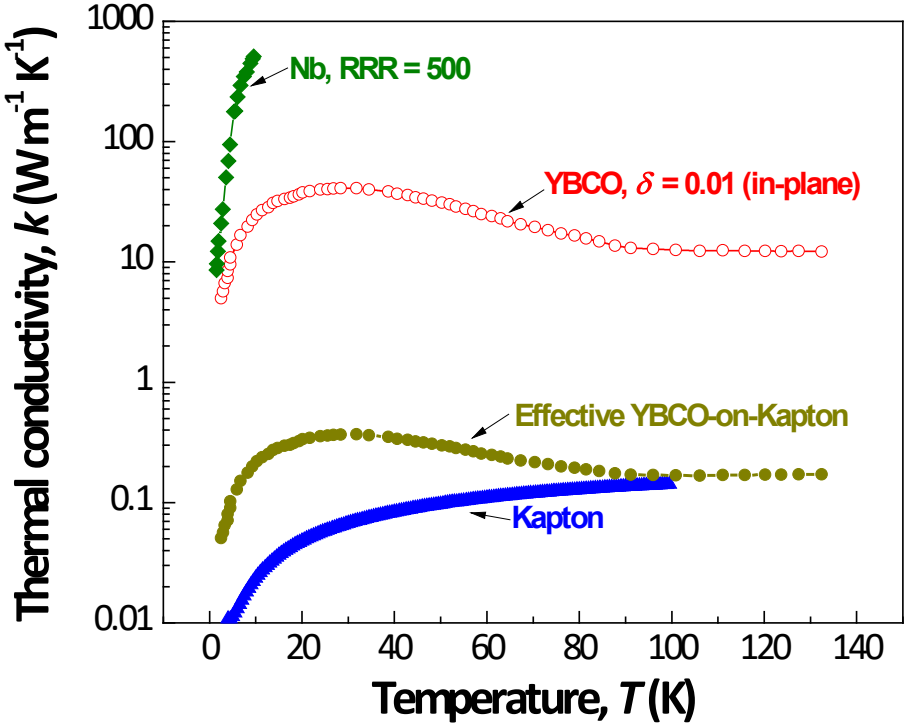


Up to 6 GHz test at Brookhaven National Lab



< 0.5 dB loss at 6 GHz

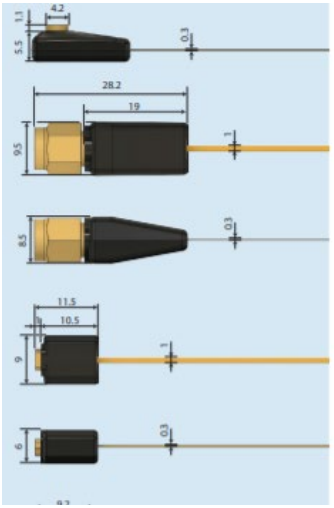
Conduction loss considerations

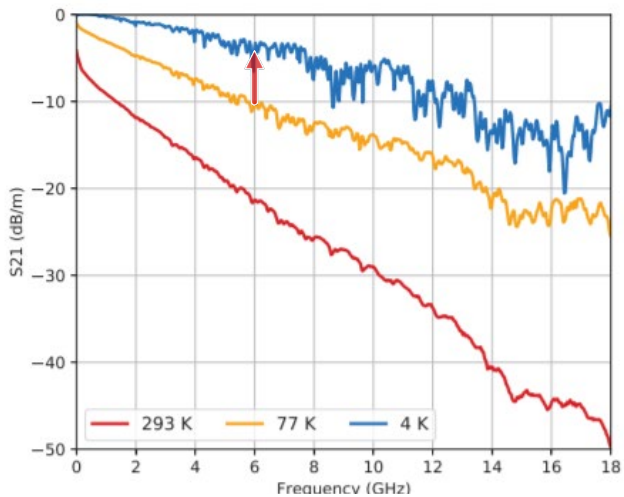


✓ **Effect of film disorder on k needs to be further investigated**

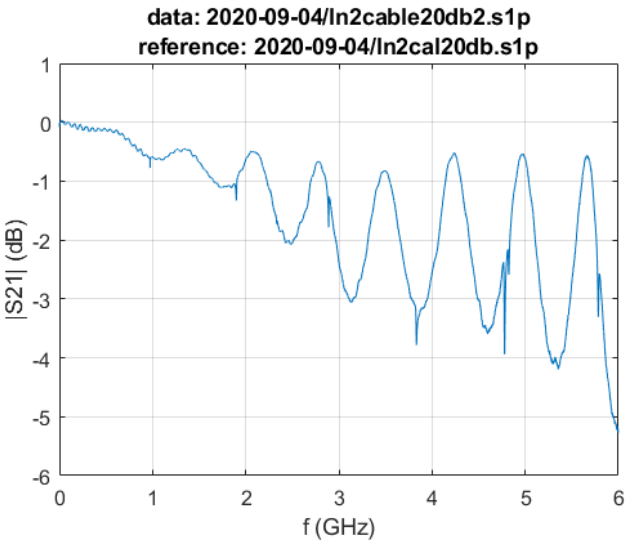
Comparison with the common metal (Ag) commercial microstrips

Ag on Kapton, CryoFlex-II, Delft Circuits



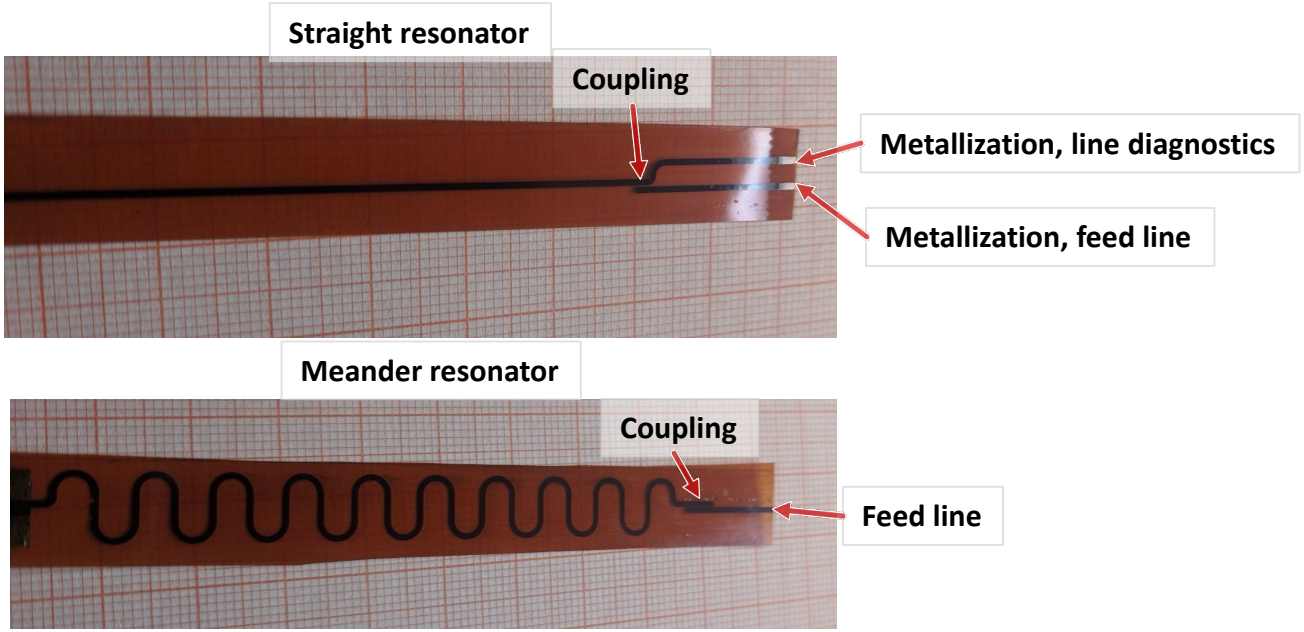


YBCO on Kapton, BTG

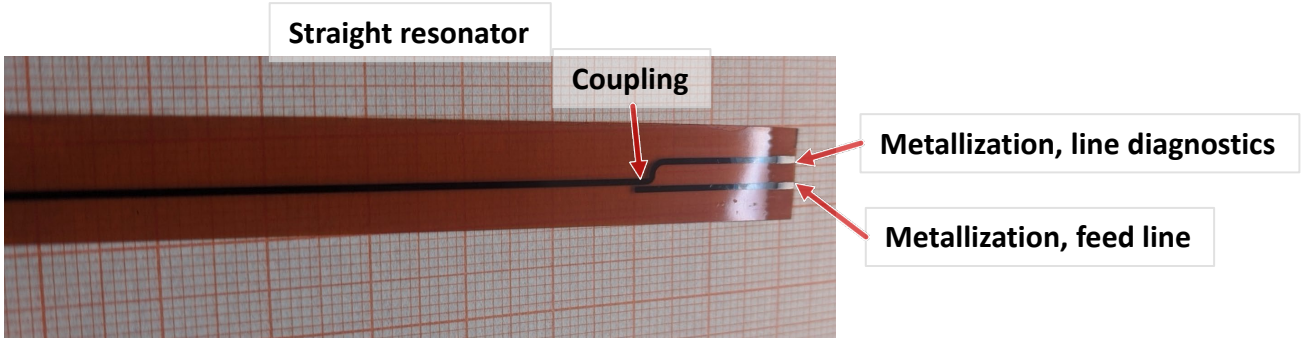


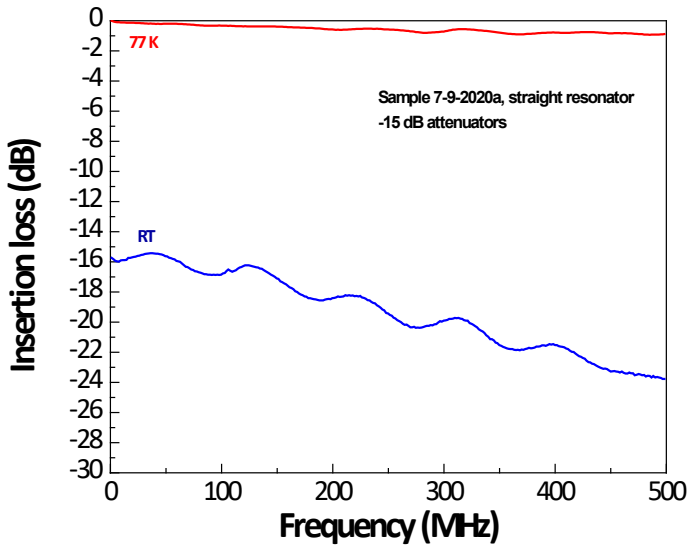
✓ **Projected 2-3 times lower loss and lower thermal conductivity**

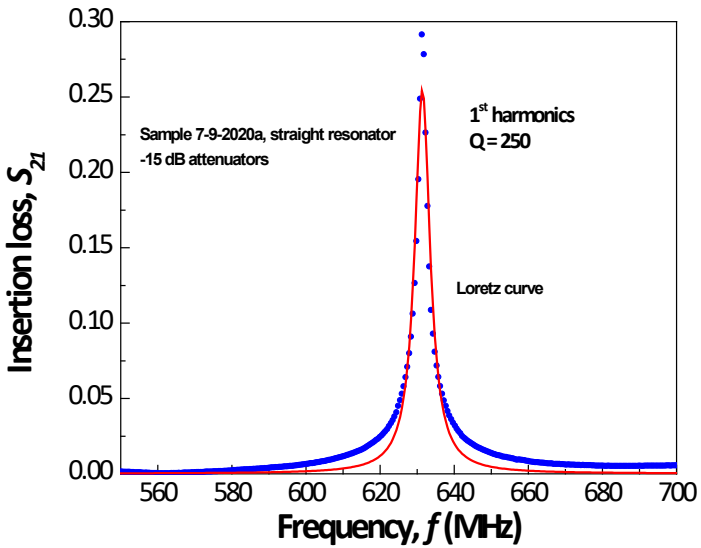
Resonator design, test of Q factor of dielectric lines



Capacitive coupled resonator, 77 K test







✓ **Quality factor 250 at 77 K at 630 MHz**

Summary

- Manufactured air-gapped and dielectric 3-filament microstrips
- Demonstrated superconducting transition in conduction-cooled mode
- Detailed insertion loss measurements up to 500 MHz at 18 K, conduction cooled
- Dielectric microstrips demonstrate < 0.5 dB loss (over 15 cm) at 6 GHz at 77 K